

EAST - [10697649.wsp:1]

File View Edit Tools Window Help

Search [] Browse [] Query []

DEF: US-CPUB; USPAT; EP ☐ Flurs

Default generator: OR ☐ Highlight all hit items and all

(deep adj trench adj dynamic adj random adj access adj memory or DT near DRAM) and (capacitor with trench) and (protrusion with bottom)

4

	U	Y	Document ID	Issue Date	Pages	Title	Current OR	Current XRef
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20040056248 A1	20040325	12	Test key for detecting electrical isolation between a word line and a deep trench capacitor in dram cells	257/48	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20040036051 A1	20040226	78	Integrated capacitor with enhanced capacitance density and method of fabricating same	251/301	257/E21.651
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20030124805 A1	20030703	7	High aspect ratio PBL SW barrier formation	438/270	438/243
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20030098483 A1	20030529	15	Vertical internally-connected trench cell (V-ICTC) and formation method for semiconductor memory devices	257/301	257/E21.652; 257/E21.653
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20030042524 A1	20030306	15	Vertical internally-connected trench cell (V-ICTC) and formation method for semiconductor memory devices	257/301	257/E21.652; 257/E21.653
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20010046745 A1	20011129	12	BITLINE DIFFUSION WITH HALO FOR IMPROVED ARRAY THRESHOLD VOLTAGE CONTROL	438/306	257/E21.345; 257/E21.437; 257/E21.651;
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20010039087 A1	20011108	16	Dram trench capacitor	438/243	257/E21.651; 438/386
9	<input type="checkbox"/>	<input type="checkbox"/>	US 6897508 B2	20050524	74	Integrated capacitor with enhanced capacitance density and method of fabricating same	257/301	361/311; 438/239; 438/71
10	<input type="checkbox"/>	<input type="checkbox"/>	US 6828615 B2	20041207	14	Vertical internally-connected trench cell (V-ICTC) and formation method for semiconductor memory devices	257/301	257/302
11	<input type="checkbox"/>	<input type="checkbox"/>	US 6677197 B2	20040113	9	High aspect ratio PBL SW barrier formation	438/245	438/244; 438/387; 438/388
12	<input type="checkbox"/>	<input type="checkbox"/>	US 6566190 B2	20030520	15	Vertical internally-connected trench cell (V-ICTC) and formation method for semiconductor memory devices	438/242	257/E21.652; 257/E21.653; 438/744

4

rt Inbox - Micr... Document3... eDAN 1.6.1... EAST - [106... EAST Brow...

BEST AVAILABLE COPY